DESIGN AND DEVELOPMENT OF FPGA BASED DIGITAL PROTECTION RELAYS FOR SMART MICROGRID

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by

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1. INTRODUCTION

After the discovery of Electricity, Power Systems have great evolution from separate units to integrated grid, where generation, transmission, distribution and load in a region were all under direct control of a single governing body. Then this system of single integrated grid changes to modern deregulated power system. Now the subsystems of generation, transmission and distribution belong to different governing bodies and therefore user has the flexibility to choose the supplier. The competition and flexibility has improved the efficiency of power systems. But at the same time, the management of physical power system in the presence of many independent companies has become quite complicated.

There are several faults namely- Single Line to Ground Fault, Line to Line Fault, Line- Line Ground Fault, Three Phase Fault, Three Phase to Ground Fault, Open Circuit Fault, etc., . These abnormal conditions often occur to the Power System. These abnormal conditions are likely to cause damage to equipment in the power system. These equipments are of heavy cost. So we have to use protective relays and circuit breakers and isolators.

Besides the evolution in power systems a corresponding evolution has taken place in the area of power system protection in general and power system relaying in particular. Relays are the first link of protection against faults and emergency conditions threatening the normal operation of the power systems. Relays have evolved from expensive electromagnetic relays to relatively cheaper solid state relays to modern digital relays which are economical, robust as well as easily adaptable to changing condition. So if the relay did not operate when it was supposed to do so, or the relay operated when it was not supposes to do so, then this will effect and disturb the users and their equipments.

Electromechanical Relays represent the first generation of relays. When the principle of electromechanical energy conversion is used for decision making, the relay is referred as an electromechanical relay (B Ram & D N Vishwakarma, [41]). Electromechanical relays work on the principle of a mechanical force generated due to the current flow in a coil wound on a magnetic core. This force results in the operation of a contact arrangement which is used for relaying the operated condition to the desired circuit in order to achieve the required function. Since the mechanical force is generated due to electric current flows, the term

‘electromechanical relay’ is used. The mechanical movement of the operating mechanism is imparted to a contact assembly to open or to close the contacts. When we say that the relay operates, we mean that it changes the state of its contacts, i.e. from Open to Close or from Close to Open. A majority of the relays are provided with a ‘control spring’ or are re-strained by gravity, so that they assume a given position when in a de-energised state. The contacts which are closed in this condition are termed as ‘normally closed’ and the ones which are open are termed as ‘normally open’. Electromechanical relays operate basically on any one of the two fundamentally different operating principles, viz. electromagnetic attraction, and electromagnetic induction. The different variety of relays, i.e. Attracted armature relays , Moving coil relays, Induction relays , Thermal relays, Motor operated relays, Mechanical relays. Electromagnetic attraction type relays operate as a result of a plunger being drawn into an electromagnet (solenoid), or an armature being attracted to the poles of an electromagnet. The electromagnetic induction relays operate on the induction motor principle wherein a torque is developed due to electromagnetic induction in a rotor. This operating principle, however, applies only to relays actuated by alternating currents.

Drawbacks of Electromechanical relays: Electromechanical relays have moving parts and also contacts so theses relays are bulk, Large in size, having Slow response due to inertia in moving parts, High maintenance, Affected by vibrations and shocks caused by external sources.

Solid State Relays represent the second generation of relays. With the advent of transistors, operational amplifiers etc., solid state relays were developed. They realize the functionality through various operations like comparators etc. They provide more flexibility and have less power consumption than their electromechanical counterpart. A major advantage with the solid state relays is their ability to provide self-checking facility i.e. the relays can monitor their own health and raise a flag or alarm if its own component fails (B Ram & D N Vishwakarma, [41]).

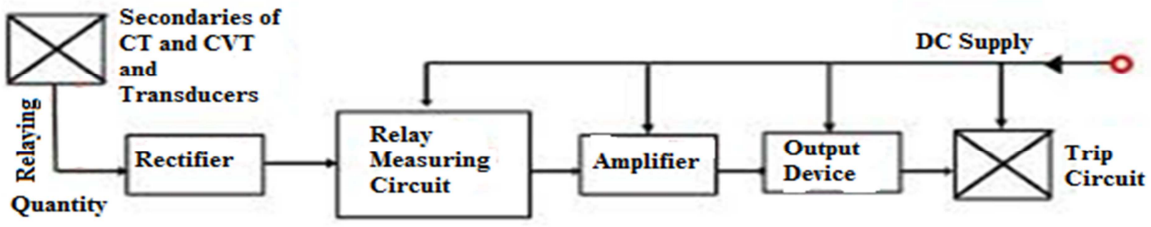

Figure1.1 Static Relay

Input Insulation Circuit provides the galvanic insulation between the input circuit and rest of the mounting while Adaptation Circuit receives the control signal and transmits it to the switching component. According to the type of relay, the making moment can take place at different levels of mains voltage. There are therefore different categories of relays. Power Switching Component used for alternating networks are thyristors or triacs. Protective Circuit used in the relays are generally RC network (snubber) or voltage protection by voltage surge suppressor. The performance of the more recent static distance relays has been so much superior to that of the electromagnetic type that power companies have been forced to accept them. Thus they may be the thin edge of the wedge of general acceptance of static relays. This would never have been achieved by time-current relays because high performance is less important in their applications. The high performance of distance relays have been achieved by advances in the design of phase and amplitude comparators.

Drawbacks of solid state relays: Solid state relays have variation of characteristics with temperature and age, No programming capability, Vulnerability to voltage spikes and high ambient temperatures, Dependence upon the reliability of a large number of small components and their electrical connections, lack of life-test data due to rapid replacement by new designs, Low short-time overload capacity compared with electromechanical relays, needs an auxiliary power supply.

Numerical Relays represent the third generation of relays. It involves analog to digital (A/D) conversion of analog voltage and currents obtained from secondary of CTs and VTs. These current and voltage samples are fed to the microprocessor or Digital Signal Processors (DSPs) where the protection algorithms or programs process the signals and decide whether a fault exists in the apparatus under consideration or not. In case, a fault is diagnosed, a trip decision is issued (B Ram & D N Vishwakarma, [41]).

With the developments in VLSI technology, sophisticated and fast microprocessors are coming up and used in digital relaying. The advantages of microprocessor-based protective relaying include flexibility, low cost, small size, and software testing aids. Since the usual relay inputs consists of power system voltage and currents, it is necessary to obtain a digital representation of these parameters. This is done by sampling the analog signals and using an appropriate computer algorithm to create suitable digital representations of the signals. In this current and voltage

signals from the power system are processed by signal conditioners consisting of analog circuits, such as transducer, surge suppression circuits and anti-aliasing filters, before sampled and converted to digital form by the analog-to-digital converter. The analog input signals are generally frozen by a sample and hold circuit, in order to achieve simultaneous sampling of all signals regardless of the data conversion speed of analog-to-digital converter. The relaying algorithm processes the sampled data to produce a digital output (Elgerd, [8]).

Advantages of numeric relays: Its ability to diagnosis itself, Communication capability, Remote diagnostics, Data sharing ability, Cost competitive, Fast speed, semi-custom application specific, parallel processing in FPGA based relays, Compact Size, Flexibility, Reliability, Multi-Function Capability, Different types of relay characteristics from single unit, Digital communication capabilities, Modular frame (consists of standard modules resulting in ease of service), Low burden on the instrument transformers, Sensitivity, Fast Resetting, Availability of fault data and disturbance record (Nature of fault, Magnitude of fault level, Breaker problem, C.T. saturation , Duration of fault etc.) Auto Resetting, Self Diagnosis.

Limitations of Numerical Relay :

i. Numerical Relay offers more functionality, and greater precision. Unfortunately, that does not necessarily translate into better protection.
ii. Numerical Relay can make faster decisions. However, in the real world, faster protection itself is of no value because circuit breakers are still required to interrupt at the direction of the protective equipment, and the ability to make circuit breakers interrupt faster is very limited.
iii. Numerical Relay protection often relies on non-proprietary software, exposing the system to potential risk of hacking.
iv. Numerical Relay protection sometimes has exposure to externally-sourced transient interference that would not affect conventional technology.
v. Numerical Relay protection shares common functions. This means that there are common failure modes that can affect multiple elements of protection. For example, failure of a power supply or an input signal processor may disable an entire protective device that provides many different protection functions. This problem has receive a lot of design

attention, and experience generally has supported the notion that the equipment has a very high reliability once it is past the infant mortality stage.

Digital Relay: Around 1980s the digital relay entered the market. Compared to the Solid State Relay, the digital relay takes the advantages of the development of microprocessors and microcontrollers. Instead of using analog signals, the digital relay converts all measured analog quantities into digital signals. These relays are a revolution step in changing Relay technology. In Digital Relay Microprocessors and micro controllers are used in replacement of analogue circuits used in static relays to implement relay functions. By the mid-1990s the solid state and electromechanical relay had been mostly replaced by digital relay in new construction. In distribution applications, the replacement by the digital relay proceeded a bit more slowly. While the great majority of feeder relays in new applications today are digital, the solid state relay still sees some use where simplicity of the application allows for simpler relays, and which allows one to avoid the complexity of digital relays.

Compared to static relays, digital relays introduce Analogue to Digital Convertor (A/D conversion) of all measured analogue quantities and use a microprocessor to implement the protection algorithm. The microprocessor may use some kind of counting technique, or use the Discrete Fourier Transform (DFT) to implement the algorithm. This relay consists of Analogue input subsystem, Digital input subsystem, Digital output subsystem, a processor along with RAM (data scratch pad), main memory (historical data file) and Power supply. Digital relaying involves digital processing of one or more analog signals in three steps: Conversion of analogue signal to digital form processing of digital form Boolean decision to trip or not to trip.

Advantages of Digital Relay: High level of functionality integration, Additional monitoring functions, Functional flexibility, Capable of working under a wide range of temperatures, can implement more complex function and are generally more accurate, Self-checking and self-adaptability, Able to communicate with other digital equipment (pear to pear). Less sensitive to temperature & aging, Economical because can be produced in volumes, More Accurate, plane for distance relaying is possible, Signal storage is possible.

Relays have been traditionally developed and evolved in the vertically integrated environment with fixed settings, predetermined coordination of primary and backup protection etc. Advent of

digital relaying has enabled more flexible approach with several advantages viz. adaptive relaying, data logging, self-diagnosis and low cost. However, there still are bottlenecks to be sorted out to keep pace with rapidly evolving modern protection schemes. The bottlenecks may be summarized as below:

1. Digital relay was developed with a 8/16 bit microprocessor its heart. This was later on replaced by more efficient microcontrollers and now DSP processors are also being used. These technologies have undergone a revolutionary change over last two decade and the resulting improvements in speed, efficiency have been successfully imparted to digital relays also. However, the fact still remains that all these processors are sequential machines. This mean all the steps in the relay viz. sensing, measurements, processing and communication of data are done sequentially. This results in a reduction in the effective sampling frequency, affecting the accuracy of all the following processes/studies. A parallel implementation would call for multiple processors with a corresponding increase in the cost as well as complexity of the relay.

2. Communication delay is the second major bottleneck. There are various modes of communication viz. dedicated microwave links, fiber optic links, satellite communication, internet etc. A dedicated fiber optic link is reported to be the best and fastest. However, even in this, the average delay is reported to be 50ms to 100 ms which is unacceptable during emergency conditions when a sub-cycle tripping is expected.

A third parallel evolution is in progress in the area of programmable hardware for implementing digital logic. The need for having programmable chips for implementing digital logic was realized in and resulted in the development of a series of such devices including PLAs, PALs, PLDs, CPLDs and FPGAs and FPAAs.

The salient advantages offered by FPGAs in the context of Power System Protection may be summarized as below:

1. FPGAs offer the advantages of parallel processing. It is possible to design concurrently operating building blocks and implement it in the form of digital circuits.

2.The design gets implemented in the form of a hardware circuits. It is possible to estimate the time delays in different modules and optimize the design for minimizing the time delays or chip area or power dissipation.

3.FPGA based design gives the ability to have a pipelined architecture where sampling, measurements, processing and communication parts can work concurrently with independent pipelines. This would increase the effective sampling frequency of the system.

4.Calculation intensive modules which cannot be conveniently represented in the form of hardware circuits may be executed by microcontroller soft cores in the same FPGA chip.

5.Recent developments in FPAAs and mixed signal chips would enable inclusion of analog designs (e.g. filters etc.) also on the same chip/board.

6.The technology is quite mature now but surprisingly it has not really percolated to power systems so far.

FPGA The FPGA is an integrated circuit that contains many (64 to over 10,000) identical logic cells that can be viewed as standard components. Each logic cell can independently take

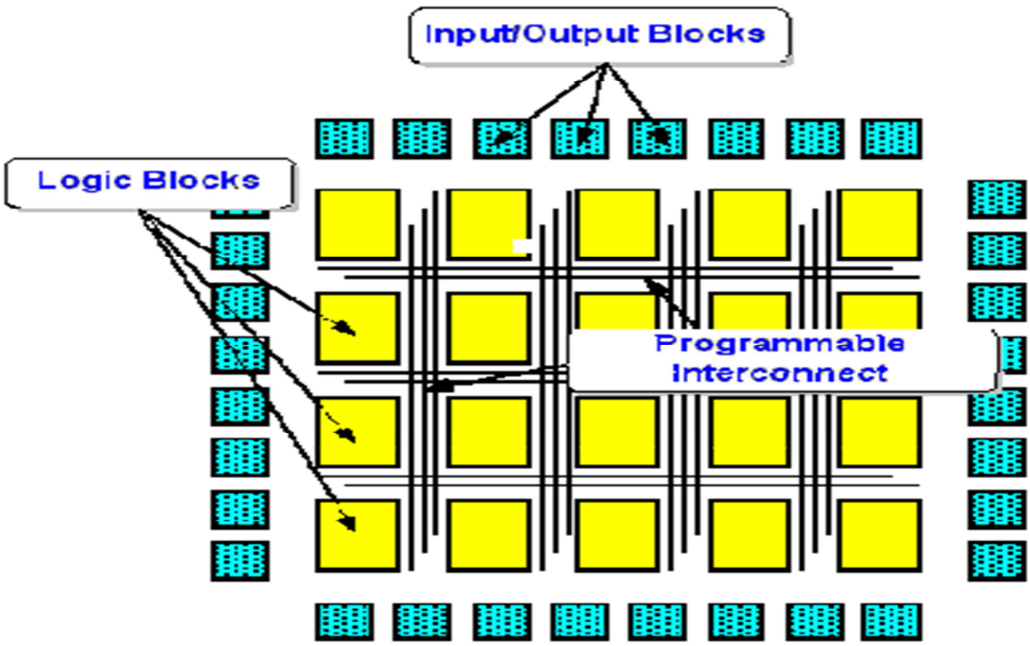

Figure 1.2 FPGA Architecture

any one of a limited set of personalities. The individual cells are interconnected by a matrix of

wires and programmable switches. The FPGA has three major configurable elements: configurable logic blocks (CLBs), input/output blocks (IOB), and interconnects. The CLBs provide the functional elements for constructing user's logic. The IOBs provide the interface between the package pins and internal signal lines. The programmable interconnect resources provide routing paths to connect the inputs and outputs of the CLBs and IOBs onto the appropriate networks.

Individually defining the many switch connections and cell logic functions would be a difficult task. Fortunately, this is handled by special software such as VHDL: Very High Speed Integrated Circuits (VHSIC) Hardware Description Language or Verilog HDL. These softwares translate a user's schematic diagrams or textual hardware description language code then places and routes the translated design. Most of the software packages have hooks to allow the user to influence implementation, placement and routing to obtain better performance and utilization of the device. Libraries of more complex function macros and different cores in these languages further simplify the design process by providing common circuits that are already optimized for speed or area.

Dependability and Security represent two conflicting attributes of a relaying scheme. To cope up with these technical issues and the same time, keeping pace with rapidly changing business scenario in power system, a number of novel relaying schemes have been proposed viz. Special/System Protection Systems (SPS) (Wright, 2013, [51]), System Integrity Protection Systems (SIPS), Remedial Action Systems (RAS), Wide area measurement Systems (WAMS) (Pal et al., 2007, [31]), Self-healing power grid (Wright, 2013, [51]) etc. which rely heavily on Modern Information and Communication Technology. It is also expected that the enabling ICT tools would eventually make it possible to implement Wide Area Protection and Control (WAPC), bringing Measurement, Relaying and Control of power systems (Zhu et al., 2011, [52]).

2. LITERATURE REVIEW

An approach for generating software models for microprocessor-based protective relays and provided illustrative test results was described by (Sidhu et al., 1998, [45]). They demonstrated the accuracy of the proposed technique, software models for an overcurrent relay and a distance relay by producing and testing them.

The digital protective relays in power distribution system were presented by (Tao et al., 2001, [46]) and (Zhang, 2001, [13]). They implemented 2 Altera FPGAs one is for measurement and other is for communication, task management and protection. They used VHDL for design the implementation. The realization of wavelet transform on FPGA device for the detection of power system disturbances was proposed by (Nelson, 2002, [10]). The proposed method starts with the software simulation of wavelet transform in order to formulate the mathematical model. This is followed by the circuit synthesis and timing analysis for the validation of the designated circuit. Then, the designated portfolio can be programmed into the FPGA chip through the download

cable. By using this technique, the time information and frequency information can be unified as a visualization scheme, facilitating the supervision of electric power signals (Huang et al., 2002, [18]).

(Maheshwari et al., 2014, [29]) presented the design and hardware implementation of an overcurrent relay on Field Programmable Gate Array (FPGA) with concurrent sense-process-communicate cycles. The implementation is based on parallel pipelined architecture where sampling, measurement, processing and communication tasks are done concurrently. The relay is implemented on Xilinx Virtex-II Pro XC2VP30-FF896-7C FPGA Board. The proposed relay conforms to IEEE standard C37.112-1996 for overcurrent relays in power systems. It had equipped with serial/IP communication capability. (Maheshwari et al., 2016, [26]) showed the pipelined architecture based PMU is implemented on Field Programmable Gate Arrays, which senses-processes-communicates at the same time. The PMU is implemented on GENESYS XILINX VIRTEX 5 XC5VLX50T FPGA board with communication facility. (Maheshwari et al., 2013, [27]) describes the hardware implementation of Digital signal processing filters on FPGAs (Field programmable gate array). Technological amelioration by Xilinx on FPGAs in the past few years has opened new paths for engineers to design various applications on FPGAs.

The advent of Special protection schemes which are also known as System Integrity Protection Systems (SIPS), Remedial Action Systems (RAS),Wide Area Protection and Control (WAPC) can be traced back to eighties when it was realized that 80% of blackouts in US were due to mal-function of the protection system (Phadke, 1998, [39]). These problems encouraged the power system engineers to pack additional functionalities in the computer relays such as synchronized measurements, adaptive relaying and embedding control functions in the protection system(Taylor et al., 2005, [47]). SPS is defined as a protection scheme that is designed to detect a particular system condition that is known to cause unusual stress to the power system and to take some type of predetermined action to counteract the observed condition in a controlled manner(Thakur et al., 2004, [24]).

A vision of self-healing power grid comprising of intelligent agent based technology is proposed by (Moslehi & Kumar, 2006, [36]). Agent tasks are coordinated via execution cycles, where an execution cycle refers to a set of related tasks executed in a temporally coordinated manner. Based on the latency of real time data acquisition, the cycles can be categorized as slow or fast. The slower cycles perform the intensive computations required for system wide coordinated controls, performance optimization and control strategies. The faster cycles address local (substation and vicinity) analytical needs to respond to rapid events using the control strategies developed by slower cycles. Higher level intelligence is more prominent in slower cycle, while lower level intelligence is dominant in the faster cycles.

Key Technology Areas for Modern Protection Schemes: The Key Technology Areas (KTAs) for the development of the modern protections schemes are outlined by National

Energy Technology Laboratory (NETL) and presented by Horowitz et al., 2010, [17]). Foremost among these KTAs will be integrated communications. The communications requirements for transmission enhancements are clear. Broadband, secure, low-latency channels connecting transmission stations to each other and to control centres will enable advances in each of the other KTAs.

- Sensing and measurements will include phasor measurement data streaming over high-speed channels.
- Advanced components, such as all forms of FACTS devices, HVDC, and new storage technologies will respond to control signals sent to address perturbations occurring in milliseconds.
- Advanced control (and protection) methods will include different line relaying schemes, adaptive settings, and various system integrity protection schemes that rely on low-latency communications (Demeter et al., 2006, [6]).
- Improved interfaces and decision support will utilize instantaneous measurements from phasor measurement units (PMUs) and other sources to derive fast simulations and advanced visualization tools that can help system operators to assess the system stability.

2.1. **Wide Area Measurement Systems**: (WAMS) is a new opportunity for system operators to monitor, operate, control and protect power systems in wide geographical area. The WAMS process can be divided into the three interconnected sub-processes; data acquisition, data delivery and data processing (Carta et al., 2009, [3]). These sub-processes are respectively performed by measurement, communication and energy management subsystems. Dynamic information of power systems helps power system operators to overcome generation, operation and planning challenges that may be resulted from system restructuring. Furthermore, it has also been shown that from the big generators to the small home equipments, WAMS systems are capable of monitoring and controlling various functions in real time.

The drivers for implementing SPSs, the functional requirements of such systems including the interface and coordination with existing protection and control equipment, and the resulting design considerations such as system architecture, Human Machine Interface (HMI), communication system robustness, performance monitoring, and system test (including commissioning, manual, and automatic test modes).

The WAMS effort is a strategic effort to meet critical information needs of the changing power system (Venayagamoorthy, 2007, [48]). The WAMS infrastructure consists of people, operating practices, negotiated sharing arrangements and all else that are necessary for WAMS facilities to deliver useful information. In recent years, PMU measurements are commercially available and are widely used in power systems. On the other hand, high speed and low cost communication systems; which are worked based on a layer model, are also well-established in power systems. As a result, the definition of WAMS is slightly different from past. Nowadays, a general definition of WAMS may be presented as follows: The WAMS combines the data provided by synchrophasor and conventional measurements with capability of new communication systems in order to monitor, operate, control and protect power systems in wide geographical area (Eissa et al., 2014, [7]).

Timely and accurate data with high resolutions holds great promise for more responsible and advanced power grid operations. The research has been focusing on design of monitoring and control scheme given the assumptions that the supporting information and communication technology (ICT) systems are capable of providing data and perform control with sufficient quality. A relatively less addressed aspect is the dependency of wide-area monitoring and control (WAMC) systems on their supporting ICT architecture which is usually a compromise between various concerns, such as data quality, interoperability, or security. Without an appropriate ICT architecture design, the projected WAMC system functionalities run the risk of being jeopardized. Analytical experiments are conducted with purposes to quantify the maximum delay and input signal's sensitivity toward delay on a typical WAMC application where the control of static var compensation (SVC) is coordinated with generator excitations using phasor measurements (Zhu et al., 2011, [52]). The characteristics of this particular control scheme, two possible ICT architectures that provide data with different qualities are compared concerning the reliability of this WAMC application. This paper concludes by proposing a generic ICT architecture, enabling efficient WAMC systems implementation in terms of data quality.

Internet of Things (IoT) technologies are pervading different application domains by relying on sensing and actuating devices that share, process and present meaningful real-world information. One of the most important of these domains is certainly the Smart Grid (SG), where the use of advanced measurement and control equipment and the diffusion of communication technologies are making an adaptive, reliable, and efficient management of the energy possible, with several new applications. (Meloni et al., 2016, [34]) focused on an IoT solution for wide area measurement systems where virtualized phasor measurement resources were presented. Such types of solutions were intended to make a programmable and smart environment fostering interoperability, reusability and flexibility of SG services.

(Pal et al, 2007, [31]) described the implemented a centralized multivariable-control algorithm is designed employing remote feedback signals considering delay in signal transmission in a real-time laboratory-based dynamic simulator. Such an algorithm is numerically intensive owing to the high controller size and the predictor that takes care of the delay in signal transmission. The

performance of the proposed controller is demonstrated by practical implementation using a rapid-prototyping controller mounted on a PC-ATX.

Protection needed a fast response to react and isolate faults. The older techniques needs to the improvement in the speed and reducing time delays. One way to reduce the delay and area of FPGAs is to employ logic cluster- based architectures, where a logic cluster is a group of logic elements connected with high-speed local interconnections. (Rose et al., 2001, [33]) empirically evaluated FPGA architectures with logic clusters ranging in size from 1 to 20, and show that compared to architectures with size 1 clusters, architectures with size 8 clusters have 23% less delay (30% faster clock speed), and require 14% less area. (Sawkar et al., 1998, [44]) proposed an algorithm for minimal-delay technology mapping for library-based designs. They show that subject graphs need not be decomposed into trees for delay minimization; they can be mapped directly as DAGs.

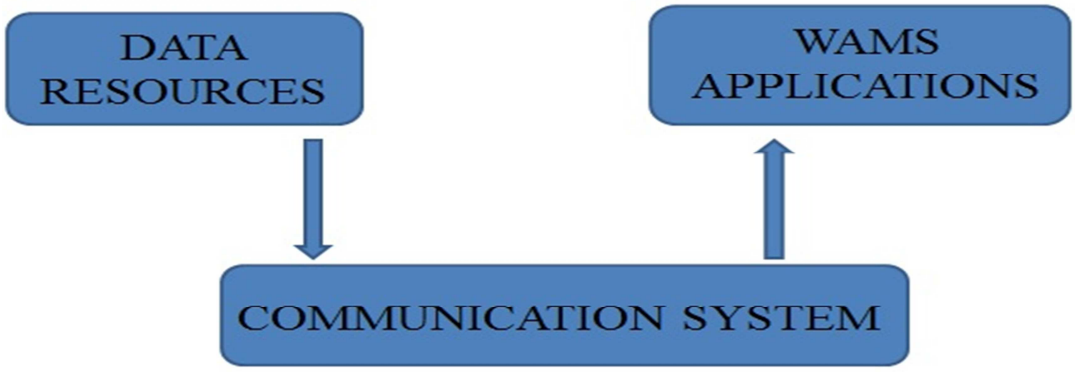

Figure 2.1 WAMS Process

2.1.1. Data resources of WAMS

Online data and information from the entire system have been essential for secure operation and control of interconnected systems e.g. power systems. In general, system data and information have been provided by data resources of system, which are also called measuring devices (Fesharaki et al., 2013, [11]). Data provided by data resources are widely different in terms of their importance, format, volume, sample rate and etc. In this section, these two classes of data resources; i.e. operational and non-operational data resources; are summarized in separate subsections. Supervisory Control and Data Acquisition (SCADA) and Synchronized Phasor Measurement System (SPMS) are two operational data resources that will be studied.

2.1.1.1. Supervisory Control and Data Acquisition (SCADA)

SCADA is a generic name for a computerized system, which is capable of gathering and processing data and applying operational controls over long distances. Typical uses of SCADA include power transmission and distribution and pipeline systems (Joshi & Ahire, 2015, [20]). In an electrical power system, a SCADA system provides three critical functions that are Data acquisition, Supervisory control, Alarm display and control in the operation of such a system.

In general, a SCADA system consists of both hardware and software. Typically, SCADA hardware may include three parts: Master Terminal Unit (MTU)[manages all communications, gathers data of RTUs, stores obtained data and information, sends information to other systems, commands system actuators that are connected to RTUs, and interfaces with operators], Remote Terminal Unit (RTU)[to control and acquire data from process equipments at the remote sites, and to communicate obtained data to a master station (MTU)], and Communication System (Joshi & Ahire, 2015, [20]). It should be noted that sometimes Programmable Logic Controllers (PLCs) [a small industrial computer, which is initially designed to perform the logic functions that are carried out by electrical equipments e.g. relays, drum switches, and mechanical timer/counters] may be used as RTU in SCADA systems.

2.1.1.2. **Synchronized Phasor Measurement System (SPMS)**: was firstly developed and introduced into the power system in mid-1980s. These systems have the ability of measuring currents and voltages, and calculating the angle between them. This ability has been made possible by the availability of Global Positioning System (GPS); on the one hand, and the sampled data processing techniques; on the other hand. In order to synchronize measured angles, SPMS uses time received from GPS as its sampling clock. In addition to measuring angles of voltages and currents, these systems can also measure local frequency and rates of frequency changes, and may be customized to measure harmonics, negative and zero sequence quantities (Phadke & Thorp, 2010, [42]). A SPMS consists of three main parts: Phasor Measurement Unit (PMU), Phasor Data Concentrator (PDC), and communication system. PMUs are normally installed at remote sites. They calculate phasors of voltages and currents and stamp measured phasors with the time received from GPS. A PDC gathers data from several PMUs, rejects bad data, and aligns the time stamps. Communication system of SPMS is responsible for data delivery between PMUs and a PDC or multiple PDCs (Phadke & Thorp, 2010, [42]). The next three sub-sections are going to describe each part of SPMS, separately.

a. **Phasor Measurement Unit (PMU)** is a microprocessor based device that uses the ability of digital signal processors in order to measure 50/60Hz AC waveforms (voltages and currents) at a typical rate of 48 samples per cycle (2400/2880 samples per second). To do this, first, the analog AC waveforms are synchronously sampled by an A/D converter for each phase. In order to provide synchronous clock for the entire system, the time from GPS satellites are used as input for a phase-lock oscillator and thereby, waveforms of the entire system are sampled with 1 microsecond accuracy. In the next step, PMU uses digital signal processing techniques to calculate the voltage and current phasors. Also, line frequencies can be calculated by PMU at

each site. By using this technique, a high degree of resolution and accuracy will be achieved. The measured phasors are tagged by GPS time stamps and are transmitted to a PDC at the rates 30-60 samples per second (Chenine & Nordstrom, 2011, [4]). Phasor data is formed in COMTRADE format (Phadke & Thorp, 2010, [42]). A study of RTU tasks in SCADA system indicates that PMU and RTU have almost the same tasks in the SPMS and SCADA systems.

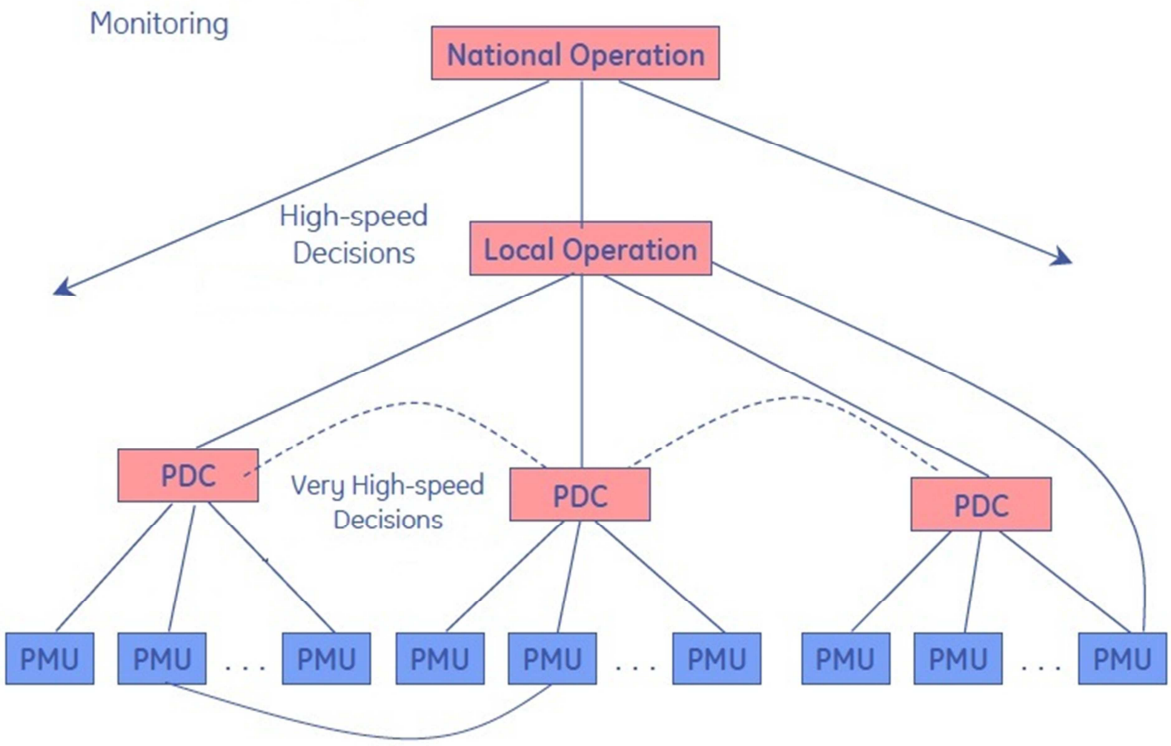

Figure 2.2 PMU Hierarchy

Phase measurement is required in electronic applications where a synchronous relationship between the signals needs to be preserved. Traditional electronic systems used for time measurement are designed using a classical mixed-signal approach. With the advent of reconfigurable hardware such as field-programmable gate arrays (FPGAs), it is more advantageous for designers to opt for all-digital architecture. Most high speed serial transceivers of the FPGA circuitry do not ensure the same chip latency after each power cycle, reset cycle, or firmware upgrade. These cause uncertainty of phase relationship between the recovered signals. To address the need to register minute phase shift changes inside an FPGA, (Nayak & Mitra, 2018, [35]) proposed a design for phase measurement logic core having resolution and precision in the range of a few picoseconds. The working principle is based on subsample accumulation using systematic sampling over the phase detector signal. The phase measurement logic can operate over a wide range of digital clock frequencies, ranging from a few kilohertz to the maximum frequency that is supported within the FPGA fabric. A mathematical model is

developed to illustrate the operating principle of the design. The VLSI architecture is designed for the logic core. They also discussed the procedure of the phase measurement system, the calibration sequence involved, followed by the performance of the design in terms of accuracy, precision, and resolution.

(Ghosh & Mohanta, 2013, [12]) investigated the impact of topological attributes on commissioning of wireless communication network for PMUs incorporating GIS aided analysis and to optimize one of the PMU location as main control station. This will not only serve for monitoring automation purposes, but will also ensure control automation. (Chenine & Nordstrom, 2011, [4]) presented the results of research performed in order to determine the requirements of transmission system operators on the performance of WAMC systems in general as well as the characteristics of communication delays incurred in centralized systems that utilize multiple PMUs distributed over a large geographic area. (Chenine & Nordstrom, 2011, [4]) presented a summary of requirements from transmission system operators with regards to a specific set of applications and simulations of communication networks with a special focus on centralized applications.

In the year 1999, (Wang et al., 2005, [50]) studied the Taipower system. They used the recent advent of synchronized Phasor measurement unit (PMU) using the global positioning system (GPS) of satellites for synchronization. They proposed PMU based SPS to prevent power system blackout due to a sequence of relay trip events. They used PMU's to monitor the generators and the major EHV transmission lines of a power system. (Abido & Al-Mohammed, 2014, [1]) presented a fully adaptive fault location algorithm for series-compensated lines (SCLs) based on synchronized phasor measurements obtained by phasor measurement units (PMUs). The SCL parameters and Thevenin's equivalent (TE) of the system at SCL terminals are determined online, utilizing three independent sets of pre-fault PMU measurements, to ensure considering the actual operating conditions of the system. Fault-location accuracy evaluation of the proposed algorithm was performed with respect to various factors such as fault position, fault type, fault resistance, fault inception angle, pre-fault loading and line compensation degree. (Abido & Al-Mohammed, 2014, [1]) simulated using both PSCAD/EMTDC and MATLAB and tested on a 400-kV system. Simulation results revealed that the developed algorithm is capable of producing reliable and highly accurate solutions.

(Qian et al., 2012, [16]) presented a fault locator for three-terminal transmission lines under dynamic conditions such as power oscillation based on synchronised phasor measurement units. Synchrophasors and frequency estimations play an increasingly important role in power systems. Therefore a dynamic phasor and frequency estimator for phasor measurement units (PMUs) was proposed by (Mai et al., 2010, [30]) to improve accuracy by considering dynamic characteristics of power systems expressed as Taylor derivatives.

Phasor measurement units (PMUs) provide the basis for synchrophasor measurements, which are good data sources for capturing power system dynamic behavior. The recently published IEEE Standard C37.118.1-2011 characterizes the dynamic performance of synchrophasor measurements with two performance class filters: P-class and M-class. Performance of an actual

PMU with the proposed reference performance class filters is presented with a brief overview of the PMU performance evaluation process and the sources of errors in the test environment. Based on the test results, some inadequacies in the reference M-class filter algorithm provided in the standard are revealed, and several minor inconsistencies in the error limits imposed by the standard are highlighted. Hence some modifications to the M-class reference filter and suggestions to rectify the minor issues in the new standard are proposed by (Narendra et al., 2014, [14]).

(Rajput et al., 2014, [40]) described a microcontroller-based phasor measurement system with Controller Area Network (CAN) bus communication capability for control of a distributed generator (DG). (Zadeh & Li, 2011, [21]) presented an adaptive transmission line auto-reclosing scheme based on synchronised phasor measurement units. Their test results show that the proposed relay is able to accurately and reliably distinguish between transient faults and permanent faults. By this discrimination, the autoreclosing is blocked during permanent fault, and the network elements could be protected from potential damages. In the case of transient faults, the proposed scheme is able to accurately detect the arc extinction time by using the voltage phasors at both ends of a transmission line and therefore prevent unsuccessful auto-reclosing during transient faults.

(Romano & Paolone, 2016, [38]) presented the literature on the subject of synchrophasor estimation (SE) algorithms has discussed the use of interpolated discrete Fourier transform (IpDFT) as an approach capable to find an optimal tradeoff between SE accuracy, response time, and computational complexity. They proposesd the formulation of an enhanced-IpDFT, the assessment of the influence of the e-IpDFT parameters on the SE accuracy, the discussion of the deployment of IpDFTbased SE algorithms into field programmable gate arrays, with particular reference to the compensation of the error introduced by the free-running clock of A/D converters with respect to the global positioning system (GPS) time reference.

(Santhosh & Bhat, 2016, [43]) discussed the implementation of a system to measure frequency, input voltage and phase of input ac signal. Quadrature sampling techniques used to measure the magnitude and phase of input signal. Frequency was measured using zero crossing detection. Modules to measure the Root Mean Square (RMS) value, phase and frequency of the input voltage were developed in Verilog HDL and implemented on Field Programmable Gate Array (FPGA). Measured values of frequency, phase and RMS voltage are displayed on Liquid Crystal Display (LCD).

(Souza et al., 2006, [5]) presented Genetic Algorithms (GAs) for measuring the frequency deviation as well as the voltage magnitude and phase angle of a noisy sinusoid wave and implemented of such a scheme in FPGA. Moreover, they investigated for the proposed GA to be implemented in FPGA simulating an online frequency relay with advantages if compared to the conventional one.

b. **Phasor Data Concentrator (PDC)**: The main functions of a PDC are: to gather data from several PMUs, to reject bad data, to align the time stamps, and to create a coherent record

of simultaneously recorded data. As a consequence, a snap-shot of phasors of the measured area can be obtained (Phadke & Thorp, 2008, [42]). In some cases, a central PDC may concentrate the area data received from other PDCs and may provide phasors of the entire system. A study of MTU tasks in a SCADA system indicates that the tasks and functions of PDC in SPMS systems are almost the same as those in SCADA systems.

(Romano et al., 2016, [38]) presented the design principles of a Phasor Data Concentrator (PDC) that implements both the absolute and relative time data pushing logics together with a third one that aims at minimizing the latency introduced by the PDC without increasing the data incompleteness. The performance of the aforementioned logics are assessed and compared in terms of reliability, determinism and reduction of the overall latency in two real Phasor Measurement Unit (PMU) installations adopting different telecom infrastructures. The first one is based on optical fiber links that transmit synchrophasor data measured by 15 PMUs installed in the sub-transmission network of the city of Lausanne, Switzerland. The second one adopts a 4G LTE wireless infrastructure to support the data streaming of 10 PMUs installed in a distribution network supplying the city of Huissen, in the Netherlands. The experimental results by (Romano et al., 2016, [38]) show that the proposed logic is characterized by the lowest latency, whereas the absolute time logic better mitigates the synchrophasor data latency variations.

2.1.2. **Communication in WAMS:** The communication systems provide communication routes between the master station and the remote sites. This can be done through private transmission media (e.g. fiber optic or leased line) or atmospheric means (wireless or satellite). There are three main physical communication architectures used in SCADA communications: point-to-point, multipoint and relay station architectures (Joshi & Ahire, 2015, [20]).

The communication systems of SPMS may be similar to the SCADA communications in terms of technology, architecture and utilized media. Although these communication systems may be the same, their streamed data are different. The phasor data, which is provided by PMUs, have different nature in comparison with the data of RTUs. Phasor data is continuous and streaming in nature while RTU data is transmitted to the master station either in a specified time intervals or when master station requests it. Another difference between PMU and RTU data is their volume. In general, data of a PMU has more value than data provided by a RTU. As a result of the above facts, two aspects are of major importance in SPMS communications: communication bandwidth and communication latency (Phadke & Thorp, 2008, [42]). High bandwidth communications guarantee that all phasor data can be transmitted to PDCs without any packet drops. On the other hand, low latency communications provide real time streaming between PMUs and PDCs.

The data transfer of Electrical System to Control Room is communicated by communication system, without which we cannot have supervision over faults and other happenings in power system. Large-scale distributed measurement systems are the object of several applications and research. (Muscas et al., 2008, [3]) proposed measurement procedures, differently from commercially available phasor measurement units, are based on general-purpose acquisition hardware and processing software, therefore promising the possibility of being easily reconfigured and reprogrammed according to the specific requirements of different possible fields of application and to their future developments. They developed measurement techniques that are suited to the continuous monitoring of the electrical quantities in distribution networks in terms of synchronized phasors, by employing Global Positioning System (GPS) receivers.
(Carta et al., 2009, [2]) also presented a measurement system, based on high-performance Global Positioning System (GPS) receivers and general-purpose acquisition (DAQ) boards, for the evaluation of the synchronized harmonic phasors in the nodes of an electric distribution network. To meet the requirements of different fields of application, they implemented two measurement procedures: One is based on a fixed observation window, whereas, in the other one, the observation interval is a function of the actual power system frequency. The phase displacement between the harmonic components of voltages and currents acquired in different nodes of an electric distribution network can be accurately measured by resorting to GPS receivers that synchronize remote acquisition systems. This leads to show that the implemented systems are able to evaluate the harmonic synchrophasors with an accuracy that meets the needs of most applications in distribution grids and to put into evidence that the input transducers, rather than the synchronized acquisition system, are the main causes of uncertainty.

2.1.1. **WAMS applications**

In general, the information about any system can be extracted from its raw data, which is measured by its data resources. In power systems, WAMS applications are classified into the three main groups: generation, transmission and distribution applications.

2.2. Digital Protective Relay (DPR)

The different kinds of protective relays have been designed to isolate the area of faults and reduce the impacts of the faults from other parts of the system as introduced in first section of this synopsis. (Bhagwan Das et al., 2014, [29]) presented the design and hardware implementation of an overcurrent relay on FPGA with concurrent pipelined architecture of sense-process-communicate cycles employed by FFT (Fast Fourier Transform) filter for isolating the fundamental component in the fault current to improve accuracy and avoid false tripping in the design. Relay has been implemented an Altera's Cylone and tested in the laboratory with encouraging results. A similar effort had also been presented by (Prabhu et al., 2006, [22]), in which the design is suitable for distribution or sub-transmission networks and can behave as extreme inverse or very inverse type of time overcurrent relay, however in both the cases the DC component filtering has not been reported which is an essential part of an overcurrent relay.

(Nabil et al., 2015, [32]) presented an efficient variant of Particle Swarm Optimization (PSO) algorithms and Time Varying Acceleration Co-efficients (PSO-TVAC) to solve optimal co-ordination of Directional Overcurrent Relays. (Hasanpour et al., 2016, [15]) solved the issue of short circuit level difference in both modes using fault current limiter (FCL). Overcurrent (O/C) relays coordination and fault current limiter impedance are selected in such a way that protection system has a suitable operation for both modes. For this purpose, artificial intelligence methods of Particle Swarm Optimization (PSO) algorithm and Cuckoo algorithm have been used to achieve optimal relays coordination and fault current limiter impedance.

(Farooq et al., 2012. [12]) presented an overview on optimal overcurrent relay coordination in protection system and protective relays. They included techniques, such as Artificial Intelligence (AI) and Nature Inspire Algorithm (NIA) as well as other conventional methods used for overcurrent protection. A brief mentioned is made about conventional methods by (Rahim et al., 2012, [19]) while more prominence is given on the application of AI and NIA for the protection of overcurrent relays.

(Natsagdorj & Erdene, 2007, [37]) studied several reasons of technical injures and fault of electrical transmission lines in Mongolia. They concluded that there is need to modify the relay protection and automation equipment.The under and overload relay helps in controlling of voltage flow, damping oscillations in voltage system, reactive voltage and transmission voltage. The controlling impedance, phase angle appropriate voltage can be varied to control the power flow. Under and overvoltage relays are used as main and back-up protection for transmission lines. The relay operates depending on ratio of voltage and current, expressed as the impedance as seen by the relay. Determining the boundary of operation of this relay is a challenging task. (Nataraj et al., 2017, [49]) and (Lee et al., 2006, [23]) present an extended review in order to identify the impact of under and over voltage on distance protection.

(Maheshwari et. al., 2015, [28]) thesis proposed FPGA based relays work on concurrent sense-process-communicate cycles therefore much fast as compare to microprocessor or microcontroller based relays. Overcurrent, impedance, reactance and mho based FPGA relays had been implemented on Xilinx Virtex-II Pro XC2VP30-FF896-7C FPGA Board and also tested on HONALEC 360 km 400 kv transmission line hardware simulator. Extraction of fundamental component of frequency is needed to avoid false tripping which was achieved with help of FFT IP core in VHDL. FFT filter is employed in implementing overcurrent, impedance, reactance and mho relay. FFT filter was also tested on DC decaying component. Very Inverse and Extremely Inverse Relay characteristics of overcurrent relay according to IEEE standard C37.112-1996 was obtained on FPGA. Distance relay viz. impedance, reactance and mho are implemented on FPGA with pipeline architecture. Test results are obtained for leading and lagging power factors for these relays when working separately and when working all together as the multifunction relay on the same FPGA board. Time delays in different pipelines viz. sense, process and communicate are calculated for overcurrent, impedance, reactance, mho and multifunction relays. Relay to relay communication was achieved. Primary relay sends signals to

secondary relay and secondary relay can take decisions based on the received parameters. In this work FPGA based relay to relay communication scheme is obtained.

It can be concluded that in modern power systems, WAMS is an essential part of power system operation and control. In particular, this text shows that dynamic information of power systems, as a result of WAMS implementation; contributes system operators to make better decisions for system operation and planning. However, in addition to the power systems, dynamic information of any interconnected system (e.g. natural gas pipelines) helps system operators/administrators to reduce operational cost and increase efficiency of such interconnected systems. Consequently, WAMS concepts may be also generalized to other interconnected systems in order to form a dynamic information system and to deliver system data to the related applications in real time. As a conclusion, it can be stated that although the WAMS was firstly introduced to the power systems in order to obtain dynamic information of such systems, it can also be well established in other critical infrastructures (e.g. natural gas, petroleum, water supply, emergency services, telecommunication and etc.) to operate, monitor and control such infrastructures.

3. Proposed Work

The thesis proposes to address the modern developments in the area of Smart Micro Grids. Specifically, the thesis proposes to investigate the following:

1. Design and development of FPGA based Wi-Fi enabled directional and overcurrent protective relays for distribution networks with special reference to Smart Micro Grids. The relays would be tested in the indigenously developed Smart Micro Grid in DEI. It is proposed to start initial design and development on FPGA development kits and finally come up with a finished product suitable for field deployment.
2. To integrate additional functionalities of metering, data logging, communication, using standard protocols in the developed relays.
3. To integrate under voltage, overvoltage, under frequency, and impedance criterions to enhance multiple functionality of the protective device.
4. To integrate the measurement of Total Harmonic Distortion (THD) up to 30^{th} harmonic to match the industry standards.
5. Design and implement special protection schemes for Renewable energy smart micro grids and implement a pilot scheme with the help of developed devices.

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